Abstract of the Disclosure

A memory array layer for use in a 3D RRAM is formed, with peripheral circuitry, on a silicon substrate; layers of silicon oxide, bottom electrode material, silicon oxide, resistor material, silicon oxide, silicon nitride, silicon oxide, top electrode and covering oxide are deposited and formed. Multiple memory array layers may be formed on top of one another. The RRAM of the invention may be programmed in a single step or a two step programming process.